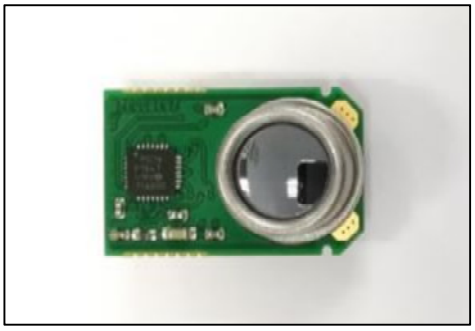
Product Specification

Thermopile Linear Array Module

TPL 32C 3774 L4.7 A60 P7 (Part Number: 9638 4320)

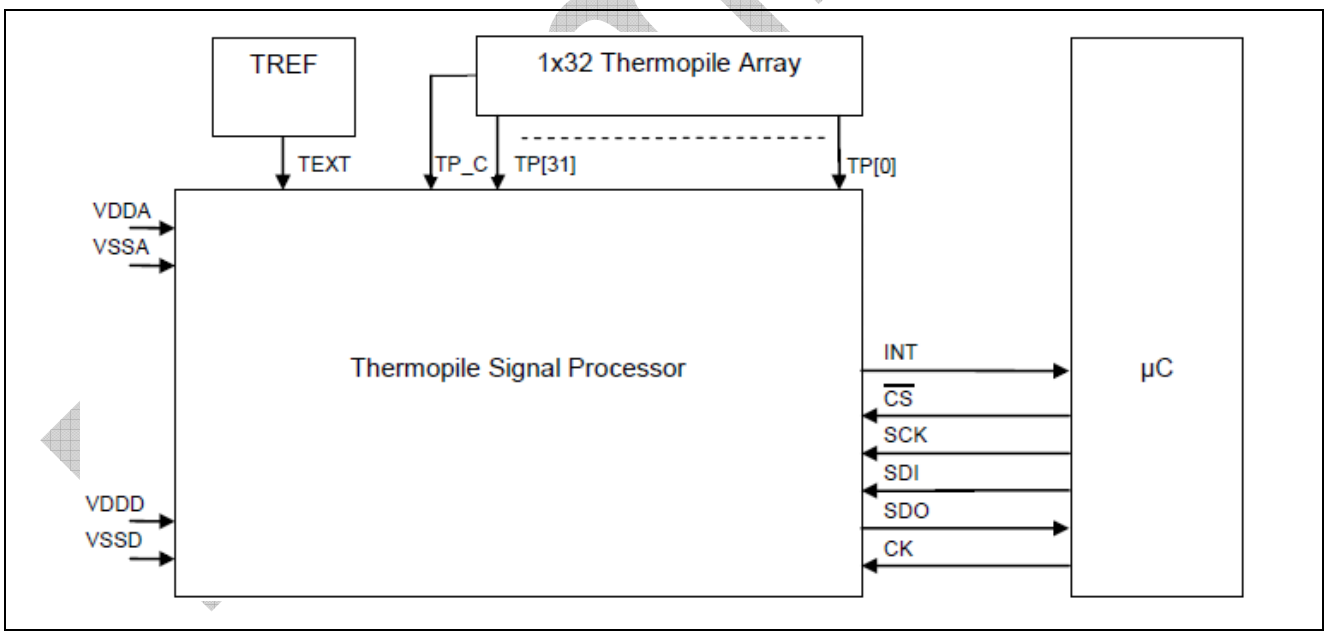
Revision 0 – Date: 2018/03/23



Product Description

The TPL 32C 3774 L4.7 A60 P7 consists of a 1x32 element thermopile chip connected to one thermopile signal processor. Each thermopile signal processor offers 32 channel ADC with digital filter and a temperature reference. The thermopile signal processors are controlled from a Microcontroller by means of SPI interface. It has a lens optic to meet the Field of View (FOV) requirements of the specific application. This module is supplied as ambient temp. compensated version and provides a calculated temperature output for each pixel.

Functional Diagram



Absolute Maximum Ratings

PARAMETERS	MIN	MAX
Storage Temperature	- 40˚C	100˚C
Operating Temperature	- 25˚C	85˚C

Electrical Characteristics

Unless otherwise indicated, all limits are specified for T_{AMB} at 25˚C, V_{DD} at 3.3V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
POWER SUPPLY						
V_{DD}	Supply Voltage	2.7	3.3	3.6	V	-
I_{DD}	Supply Current	-	-	20	mA	-
SERIAL INTERFACE (SDAT & SCLK)						
V_{iL}	Low level input voltage	-	-	0.2 * V_{DD}	V	Fall edge
V_{iH}	High level input voltage	0.8 * V_{DD}	-	-	V	Rising edge
V_{oL}	Low level output voltage NOTE 1	-	-	0.1	V	I_{Sink} = 2mA
V_{oH}	High level output voltage	V_{DD} – 0.1	-	-	V	I_{Source} = 2mA

NOTE 1: SDAT and SCLK pins have drain output.

Temperature Sensing Range

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
CALIBRATION SETTINGS						
T_{OBJ}	Calibrated object temperature range	10.0	-	60.0	˚C	Emissivity at 99.9%
$RESOLUTION_{TOBJ}$	Resolution of object temperature	0.5	-	-	˚C	-
T_{AMB}	Calibrated ambient temperature range	0.0	-	70.0	˚C	
$RESOLUTION_{TAMB}$	Resolution of ambient temperature	0.5	-	-	˚C	-

AC Characteristics

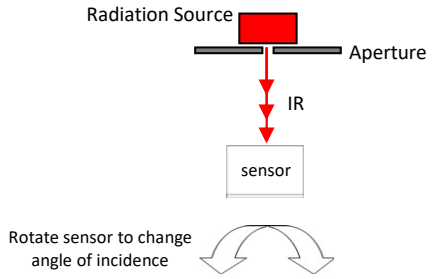
Unless otherwise indicated, all limits are specified for T_{AMB} at 25˚C, V_{DD} at 3.3V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{start}	Module time to response after power ON	-	-	500	ms	-
$t_{latency}$	Latency time for T_{OBJ}	-	190	-	ms	Default Averaging Loop Setting (Please refer to Page #8)
$t_{pix\_refresh}$	Pixel signal refresh time	-	190	-	ms	Default Averaging Loop Setting (Please refer to Page #8)
$t_{ptat\_refresh}$	PTAT signal refresh time	-	-	90	ms	Default Averaging Loop Setting (Please refer to Page #8)
AMPLIFIER						
O_N	Output noise			12	counts	Applicable for $Vpixnorm_i$ at Tobj = 25°C Default Averaging Loop Setting (Please refer to Page #8)
SERIAL INTERFACE						
f_{SMB}	Operating frequency	10		100	kHz	Please refer to Page #6 for specific conditions applicable
EEPROM						
	Data retention time	10			Years	Max T_{AMB} at 85˚C

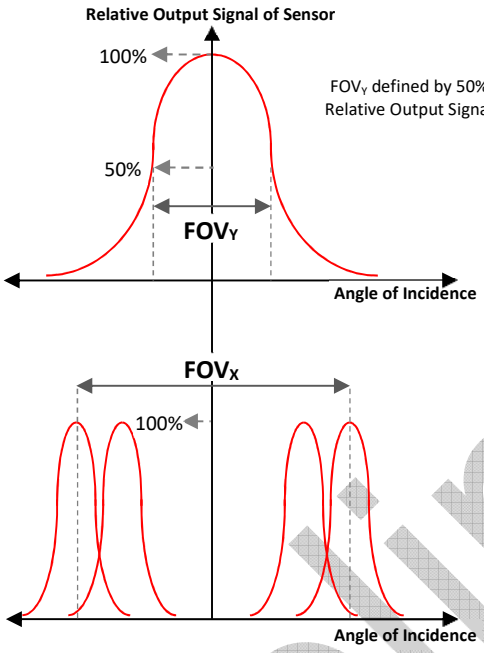
Optical Characteristics

Method of FOV Characterisation

FOV: Field of View



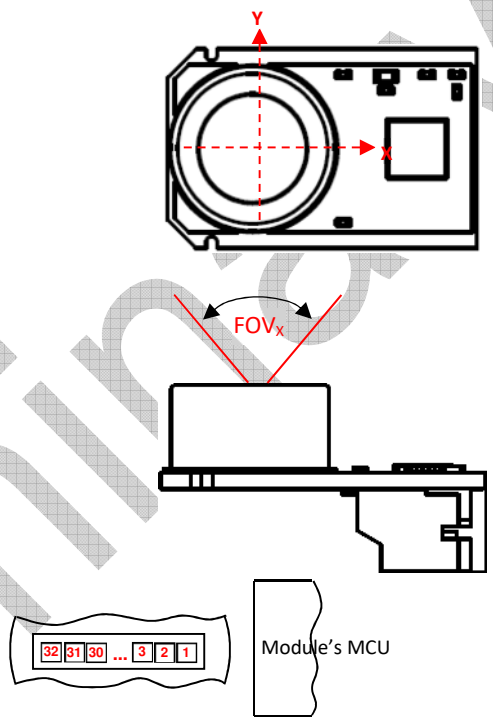
Definition of FOV



The sensors' optic defines the Field of View (FOV) of the sensor.

FOV_X is defined as the incident angle difference between peak signal position of Pixel 1 and Pixel 32.

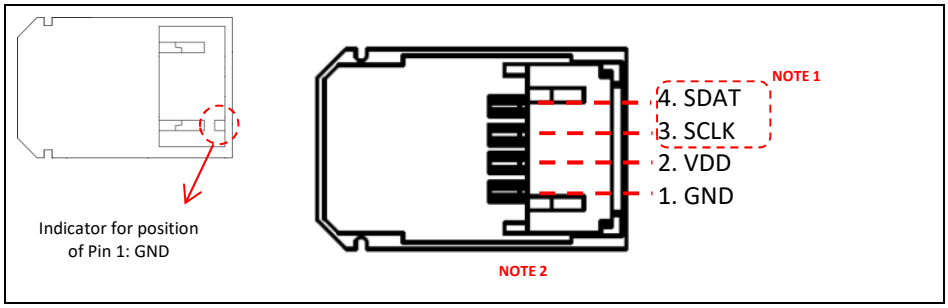
The FOV_Y is defined as the incident angle difference, where the sensor relative output signal is at 50% as shown in diagram on the left.

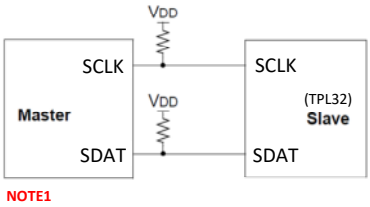


Pixels' Orientation

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
CAP TYPE L4.7						
FOV_X	Field of View X Direction	55	59	63	°	Please refer to above
FOV_Y	Field of View Y Direction	1.5	3	4.5	°	Please refer to above
OA	Optical Axis	- 6.5	0	6.5	°	-
LENS TRANSMISSION						
Average Transmission			52		%	Wavelength from 5.5µm to 13.5µm

Connection Information





NOTE 1: The SCLK and SDAT pins are open collector. Apply appropriate pull up resistors on the SMBus master device.

NOTE 2: Module connector employed: CVILUX CI0104M1HR0-LF or JST S4B-PH; or equivalent.

Serial Interface: SMBus & Data Communication Information

A '2-wire', bi-directional SMBus compatible serial interface is provided for communication of sensors' data to and from target applications.

TPL32 Application Note: SMBus Communication, provides examples to understand and to operate the SMBus communication protocol. For complete SMBus specification, please refer to the following webpage:
www.smbus.org/specs

There are 2 types of memory in the TPL32 device:

1. EEPROM – holds configuration data
2. RAM – holds temperature data.

Only READ operation is applicable to RAM data; READ / WRITE operations are applicable to EEPROM data.

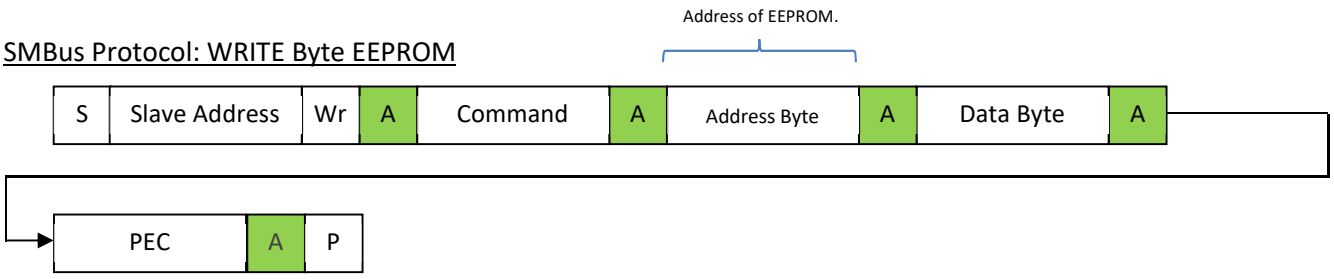
The following sub-sections specify the SMBus protocol required to: (1) WRITE Word, and (2) READ Word; according to legend provided here.

S SMBus START Condition
Sr SMBus Repeated START Condition
Rd READ (bit value 1)
Wr WRITE (bit value 0)
A ACKNOWLEDGE (ACK)
Ā NOT ACKNOWLEDGE (NACK)
P SMBus STOP Condition
PEC Packet Error Code (CRC: Cyclic Redundancy Check) please see below

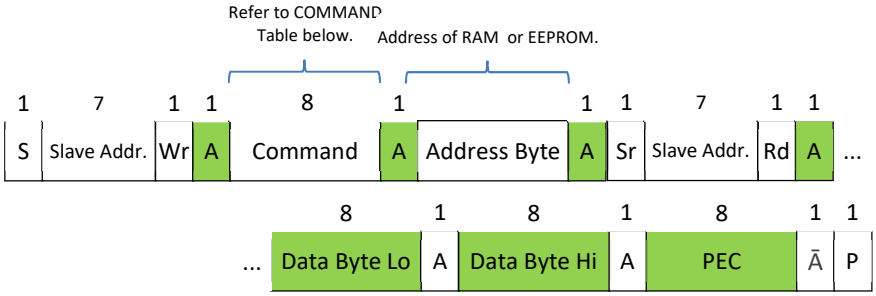
Data Direction: MASTER send to SLAVE

Data Direction: SLAVE send to MASTER

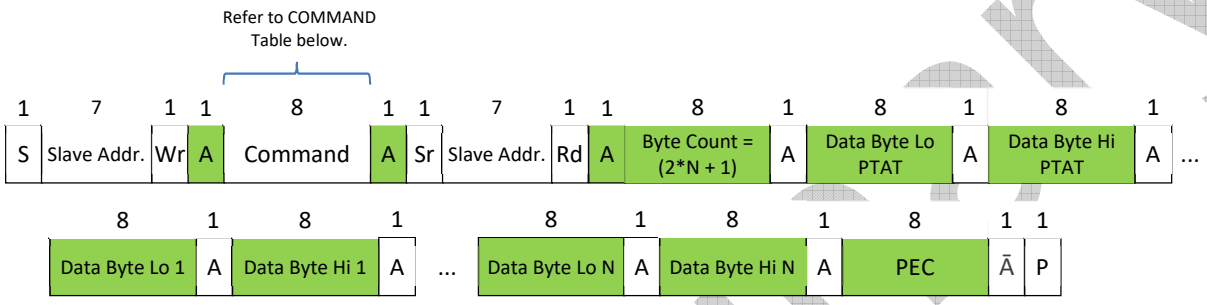
SMBus Protocol: WRITE Byte EEPROM



SMBus Protocol: READ Byte EEPROM / Word RAM (SMBus Process Call with PEC page #31 of SMB Spec. ver. 2.0)



SMBus Protocol: Block Read RAM (SMBus Block Read with PEC page #32 of SMB Spec. ver. 2.0)



COMMAND

COMMAND is a byte used by the MASTER device to tell the TPL32 what data it required. The COMMAND has the following format:

(COMMAND)	DESCRIPTIONS
0x01	Read WORD RAM
0x81	Read/Write BYTE EEPROM
0x02	Block read all pixels including internal temperature sensor
0x03	Block read of all pixels with even address including internal temperature sensor
0x04	Block read of all pixels with odd address including internal temperature sensor

NOTE: Addresses of RAM & EEPROM are described in the sections: **OUTPUT DATA INFORMATION** and **CONFIGURATION PARAMETERS & DESCRIPTIONS**

ADDRESS & BYTE COUNT

ADDRESS is a byte/word used by the MASTER device to tell the TPL32 what specific data it wants to read/write:

1. **WRITE EEPROM** – Address is one BYTE long and defines the address of EEPROM cell which the MASTER wants to write one BYTE of data to; in the WRITE EEPROM protocol.
2. **READ EEPROM** – Address is one WORD long and defines the address of EEPROM cell which the MASTER wants to read data from in the READ EEPROM protocol. Since the address and data of EEPROM of the TPL32 are not larger than one BYTE, the high byte of both address and data will normally be 0.
3. **READ RAM** – Address is one WORD long and defines the address of RAM which the MASTER wants to read data from. The descriptions of respective RAM addresses are defined on page #8.

BYTE COUNT reflects the number of following bytes which the TPL32 will transmit to the MASTER, including PEC in Block Read protocol. For example when reading all pixels BYTE COUNT = 2*33 + 1 = 67.

PEC: CYCLIC REDUNDANCY CHECK

Each bus transaction requires a Packet Error Code (PEC) calculation by both the MASTER and the SLAVE devices to ensure physical correctness of transmitted data. The PEC includes all bits of a transaction except the START, REPEATED START, STOP, ACK, and NACK bits.

The PEC employed by TPL32 is a CRC-8 with polynomial PEC = x8+x2+x1+1 = 107hex and must be calculated in the order of the bits as received.

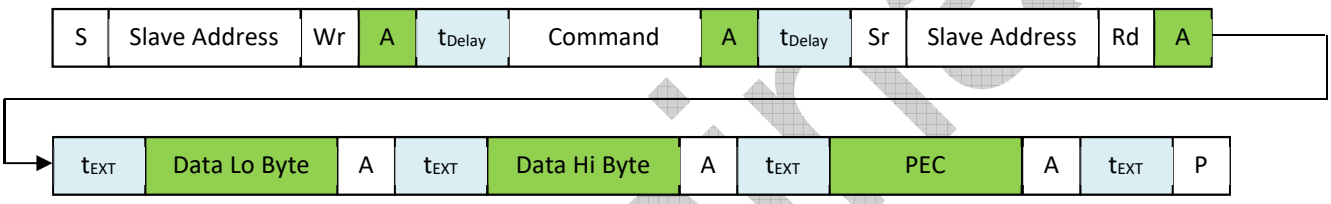
CLOCK LOW EXTENSION & DATA PREPARATION TIME

The TPL32 uses clock low extension, t_{EXT} where necessary in order to extend the low period of SCLK in order to gain time for data processing, or data preparation for transmission.

For this reason, there are also minimum timing conditions represented by data preparation time, t_{Delay} required to ensure reliable SMBus communication with the TPL32.

The diagram below shows the READ Word command as an example. In order to ensure stable SMBus communication, the MASTER Device may apply t_{Delay} time delays as indicated.

NOTE: t_{EXT} is generated automatically by TPL32, therefore Master Device do not need to apply time delay for these.



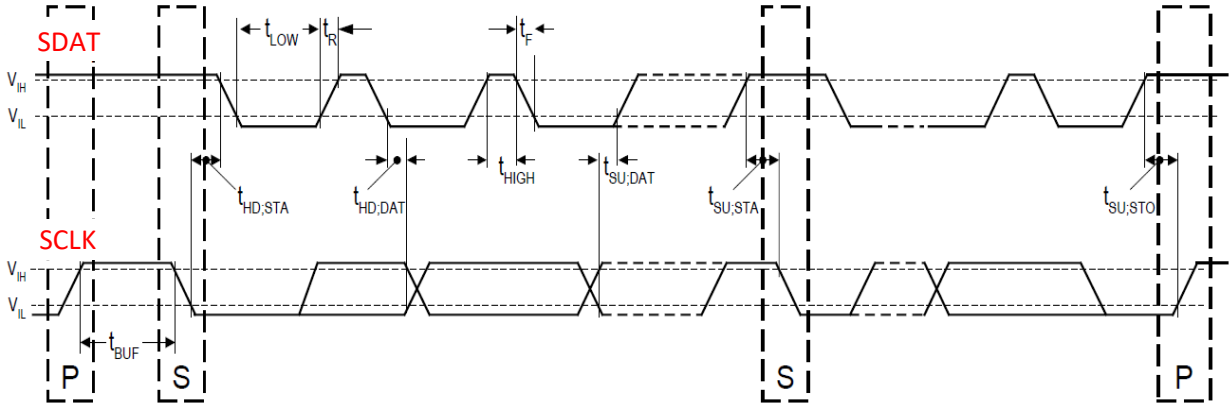
The following table provides the required settings for t_{BUF}, t_{EXT1}, t_{EXT2} and t_{Delay} at specified SCLK frequency:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{EXT}	SCLK Low Extend Time	4.7	-	-	µs	
$t_{LOW:SEXT}$	Cumulative clock low extend time (slave device)	-	-	25	ms	Sum of all t_{Delay} & t_{EXT}
t_{Delay}	Delay time between 2 Bytes to ensure proper communication	-	-	150	µs	SCLK Frequency = 100kHz

SMBus Timeout

TPL32 provides a Time-out mechanism for SMBus communication self-recovery in the event that the SMBus protocol sequence is interrupted or disturbed. Every time a new SMBus transaction is recognized by a Slave Address match, a timer is activated. If the subsequent SMBus protocol events do not occur within a span of 30ms, a Timeout occurs and as a reaction the SMBus communication sequence will be reset to be ready for a new transaction.

SMBus Signals: Timing Characteristics



Unless otherwise indicated, all limits are specified for T_{AMB} at 25˚C, V_{DD} at 3.3V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{BUF}	Bus free time between STOP and START condition.	10			µs	
$t_{HD:STA}$	Hold time after (Repeated) START Condition. After this period, the first clock is generated.	4.0			µs	
$t_{SU:STA}$	Repeated START Condition setup time.	4.7			µs	
$t_{SU:STO}$	STOP Condition setup time	4.0			µs	
$t_{HD:DAT}$	Data hold time	300			ns	
$t_{SU:DAT}$	Data setup time	250			ns	
t_{Low}	Clock low period	4.7		30000	µs	NOTE 1
t_{HIGH}	Clock high period	4.7		50	µs	NOTE 1
t_F	Clock / Data fall time			300	ns	
t_R	Clock / Data rise time			1000	ns	

NOTE 1: Refer to SMBus Timeout.

Output Data Information

Temperature outputs of the TPL32 are updated into the RAM memory. The address(s) of the RAM Data are defined by the following Table:

RAM ADDRESS	BIT	DATA	DESCRIPTION OF DATA	Value Range
0	15 … 0	**T_{AMB}**	**Calculated Ambient Temperature:** **Value = 10 * T_{AMB} [in ˚C]**	0 … 65535
1 … 32	15 … 0	**$T_{OBJ[1 \dots 32]}$**	**Calculated Object Temperature (T_{AMB} Compensated):** **Value = 10 * T_{OBJ} [in ˚C]**	0 … 65535
65	15 … 0	Tamb_VAL (PTAT)	PTAT raw data _ ADC-value	0 … 65535
66 … 97	15 … 0	$VPIX_{[1 \dots 32]}$	TP pixel raw data _ ADC-values	0 … 65535

NOTE: The data of RAM ADDRESS 65 to 97 is used for factory calibration only and not relevant for customer application.

NOTE 1: Negative temperature output are represented as follows, eg. -5°C → 65535 – 50 = 65485.

NOTE 2: Accuracy for T_{OBJ} between 25°C and 60°C are measured in Excelitas Lab. For T_{OBJ} below 25°C, accuracy is estimated.

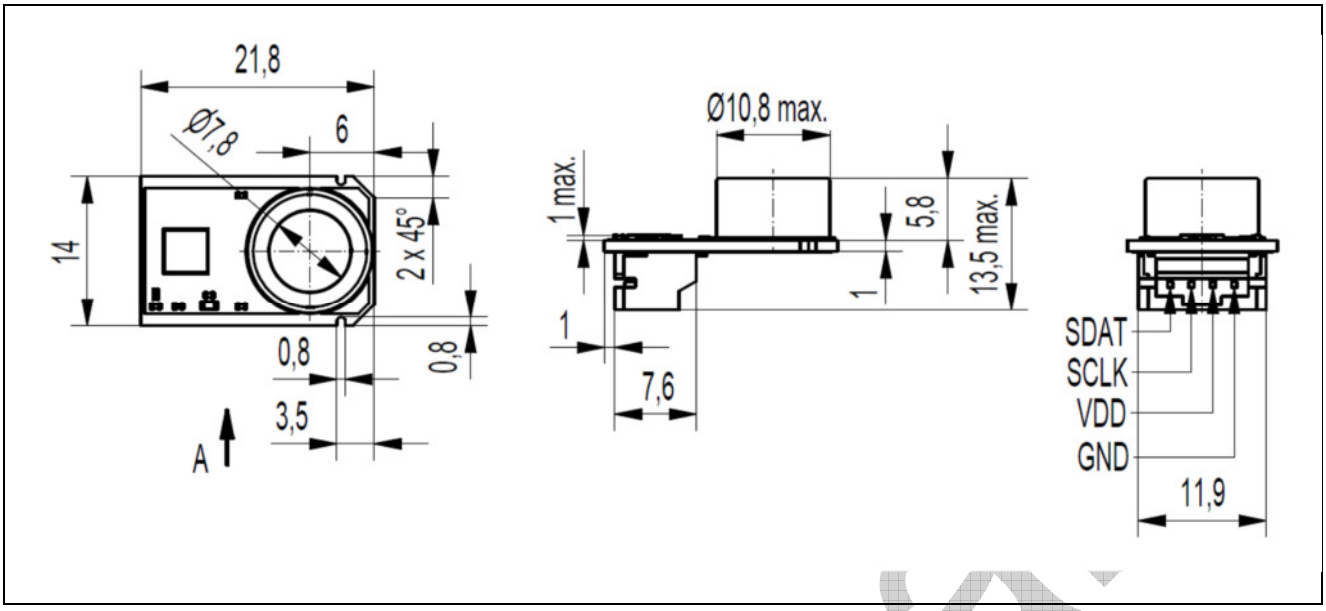
Configuration Parameters & Descriptions

The address(s) of customer accessible EEPROM Data are defined by the following Table:

EEPROM Address (MSB, LSB)	Bits	Name	Meaning	Mode	Value Range
0, 1	15 … 0	ID[NOTE 3]	Unique Sensor ID identical to corresponding sticker label applied on module	R/W	0 … 2^{16}
4, 5	6 … 0	SA	Unique SMBus Slave Address	R/W	0 … 127 (Default = $0A_{Hex}$)
	15 … 7	-	Not used	-	0
8, 9	15 … 0	DEV-Typ	e.g. option to Set Tamb temp. compensation : 4 = comp. ON (Bit 3 = 1) 0 = comp. OFF (Bit 3 = 0)	R/W	NA
12, 13	15 … 0	AVG_Count	Number of ADC samples to be averaged per frame	R/W	(Default = 13) (NO Averaging = 1)

NOTE 3: ID may not apply for engineering samples.

Mechanical Information



Soldering

The TPL32 is a lead-free component and fully complies with the RoHS regulations, especially with existing roadmaps of lead-free soldering.

NOTE: This may not apply for engineering samples.

Quality System

Excelitas Technologies is an ISO 9001 certified manufacturer. All devices employing PCB assemblies are manufactured according to IPC-A-610 guidelines.

The PCB assembly and components are of lead-free type, compliant to RoHS.

Liability Policy

The contents of this document are subject to change without notice and customers should consult with Excelitas Technologies sales representatives before ordering. Customers considering the use of Excelitas Technologies thermopile devices in applications where failure may cause personal injury or property damage, or where extremely high levels of reliability are demanded, are requested to discuss their concerns with Excelitas Technologies sales representatives before such use. The Company's responsibility for damages will be limited to the repair or replacement of defective product. As with any semiconductor device, thermopile sensors or modules have a certain inherent rate of failure. To protect against injury, damage or loss from such failures, customers are advised to incorporate appropriate safety design measures into their product.